

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,907,593 B1
DATED : June 14, 2005
INVENTOR(S) : Steven Teig et al.

Page 1 of 1

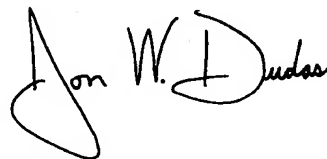
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page.

Item [57] **ABSTRACT**, reads "Some embodiments provide a method of pre-computing attributes of routes for nets in a region of a design layout. The pre-computed attributes are used by an electronic design automation application that partitions a design-layout region into a plurality of sub-region." and should read -- A method for pre-computing net route attributes for a region of an integrated circuit (IC) is presented. In one embodiment, the pre-computed attribute is the intersect cost associated with a group of previously indentified sub-region edges. In another embodiment, the pre-computed attribute is the usage cost associated with a group of previously identified sub-region paths. Such pre-computed numbers may be used by an electronic design automation application that indentifies routes for nets in the IC region. --.

Signed and Sealed this

Twenty-first Day of March, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, sweeping initial "J" and a distinct "D".

JON W. DUDAS
Director of the United States Patent and Trademark Office